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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,981	02/05/2001	Ming-Hau Lee	MORPH1140	2432

7590 02/17/2004

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EXAMINER	
CHANG, ERIC	

ART UNIT	PAPER NUMBER
2116	3

DATE MAILED: 02/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/776,981	LEE ET AL.	
	Examiner	Art Unit	
	Eric Chang	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,205,537 to Albonesi.

4. As to claim 5, Albonesi discloses a method for saving power in a processor array by:

[a] enabling a subset of cells in the array [col. 8, lines 1-18];

[b] activating each enabled cell to execute an instruction [col. 4, lines 24-35, and col. 8, lines 1-7];

[c] disabling each cell not enabled such that the disabled cell does not consume power [col. 8, lines 25-31].

Albonesi teaches enabling a subset of hardware elements, such as cells, in a processor array by control means in order to use the selected cells to execute the instructions in an application. Furthermore, Albonesi teaches that the selection of the active hardware elements is made in order to reduce power consumption, substantially as claimed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4 and 6-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,205,537 to Albonesi, in view of U.S. Patent 4,907,148 to Morton.

7. As to claim 1, Morton discloses a method for conserving power in a processor array by:

[a] enabling selected cells in a processor array by control signal means [col. 8, lines 1-18]; and

[b] enabling selected cells in said processor array in accordance with a clock signal [col. 8, lines 1-7].

Albonesi teaches that the processor array can be dynamically altered to meet the demands of each instruction in the instruction stream. Therefore Albonesi teaches that the processor array may activate and deactivate cells per clock cycle; it would be obvious to one of ordinary skill in the art that the reconfiguration would likewise be gated to the clock signal that also drives the instruction stream. Albonesi teaches all of the limitations of the claim but does not teach that the control signals comprise a row and column mask signal.

Morton teaches that providing a row and a column mask signal to enable selected cells in the array [col. 3, lines 20-51].

At the time that the invention was made, it would have been obvious to a person of ordinary skill in the art to employ the row and column masking means as taught by Morton. One of ordinary skill in the art would have been motivated to do so that cells within the processor array can be selectively enabled and disabled.

It would have been obvious to one of ordinary skill in the art to combine the teachings of the cited references because they are both directed to the problem of reconfiguring a processor array by control means. Moreover, the row and column masking means taught by Morton would improve the flexibility of Albonesi because it specifies the means by which the control registers select the cells within the processor, substantially as claimed.

8. As to claims 2-3 and 10, Albonesi discloses that only the cells required to execute a given instruction are enabled [col. 8, lines 1-18], substantially as claimed.

9. As to claim 4, Albonesi discloses updating the row and column mask signal during each clock cycle [col. 8, lines 1-7]. Albonesi teaches that the processor array can be dynamically altered to meet the demands of each instruction in the instruction stream. Therefore Albonesi teaches that the processor array may activate and deactivate cells per clock cycle; it would be obvious to one of ordinary skill in the art that the reconfiguration would likewise be gated to the clock signal that also drives the instruction stream.

10. As to claim 6, Albonesi and Morton teach a method for conserving power in a processor array by gating a row and a column mask signal to activate selected cells within the array each clock cycle. Because Albonesi and Morton teach the method, Albonesi and Morton also teach the arrangement for a processor array implementing said method, substantially as claimed.

11. As to claims 7-8 and 13, Morton discloses the row and column mask registers are M-bit and N-bit registers [col. 1, lines 49-52, and col. 3, lines 31-36], wherein the masks correspond to the rows and columns in the processor [col. 3, lines 39-51]. It would further be obvious to one of ordinary skill in the art that the mask signals from such registers would have M-bit and N-bit width, substantially as claimed.

12. As to claim 9, Morton discloses a mask generator for generating the signal to the row and column mask registers [FIG. 1, element 15, and col. 3, lines 20-31].

13. As to claim 11, Albonesi and Morton teach an arrangement for a processor array for conserving power in a processor array by gating a row and a column mask signal to activate selected cells within the array each clock cycle. Because Albonesi and Morton teach the arrangement, Albonesi and Morton also teach the circuits for generating the signals to implement said method, substantially as claimed.

14. As to claim 12, Morton discloses a row and column mask register connected to a row and column of cells, respectively [FIG. 1, and col. 3, lines 20-51].

15. As to claim 14, Morton discloses the row and column signals are gated together at an input to each cell [col. 3, lines 39-51]. Morton teaches that the cells at the intersection of the row and column signals are enabled and disabled according to said signals.

16. As to claim 15, Morton discloses the mask signal is configured to enable the masked cells [col. 3, lines 39-51].

Conclusion

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Chang whose telephone number is (703) 305-4612. The examiner can normally be reached on M-F 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 6, 2004
ec

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